



Astera Labs Expands Global Footprint with New Israel Design Center to Support Growing Demand for AI Connectivity Solutions

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New design center to focus on cutting-edge AI fabrics and emerging AI inference technologies

Industry veteran Guy Azrad to lead operations as general manager of Astera Labs Israel

SAN JOSE, Calif. and TEL AVIV, Israel, Feb. 09, 2026 (GLOBE NEWSWIRE) -- Astera Labs, Inc. (Nasdaq: ALAB), a leader in semiconductor-based connectivity solutions for rack-scale AI infrastructure, today announced a significant expansion of its global engineering operations with the establishment of an advanced research and development center in Israel. The new design center will accelerate the development of Astera Lab's next-generation scale-up fabrics for high-bandwidth connectivity protocols, while also advancing technical research and development to address memory bottlenecks in AI training and inference applications. Semiconductor industry veteran Guy Azrad, senior vice president of engineering and general manager of Astera Labs Israel, will lead the new Israel operations, and will be supported by Ido Bukspan as vice president of ASIC engineering.

Astera Labs is expanding its global engineering footprint with the new Israel design center as a strategic investment in one of the world's premier semiconductor ecosystems. The new center creates an end-to-end facility for advanced research and development of connectivity solutions in Israel that aims to solve critical data, network, and memory bottlenecks. Through collaborations with leading Israeli universities and the venture ecosystem, the design center is expected to serve as a hub to advance technologies critical to support next-generation AI infrastructure worldwide.

"We're building an engineering team with a strong focus on execution, covering hardware, silicon, and software solutions, to support the growing adoption of Astera Labs' Intelligent Connectivity Platform," said Guy Azrad, senior vice president of Engineering and general manager of Astera Labs Israel. "With offices in Tel Aviv and Haifa, the new Israel design center will look to tap into the region's world-class engineering talent to focus on the full chip design flow—from architecture through production, including software and system design for cutting-edge AI fabrics and emerging inference applications."

Guy Azrad brings extensive semiconductor leadership experience in high-speed networking, compute, and Ethernet technologies to his role as general manager of the Israel design center. He most recently served as vice president of chip design engineering at Google, where he led silicon development for compute applications. Prior to Google, he held senior engineering leadership roles at Marvell, where he was senior vice president of the company's global Ethernet switching division, overseeing development of advanced networking solutions deployed across data centers worldwide. His career spans deep expertise in developing advanced networking system-on-chips (SoCs), building and scaling large-scale chip design organizations across multiple geographies, and delivering complex silicon solutions from architecture through production. Azrad has been instrumental in bringing multiple generations of high-performance networking products to market.

The Israel design center expansion is further strengthened by the addition of Ido Bukspan, who joins Astera Labs as vice president of ASIC Engineering to support the company's scale-up fabric development initiatives. Bukspan brings over two decades of networking and semiconductor expertise from his combined tenure at Mellanox Technologies and NVIDIA, where he spent 20+ years and rose to the position of senior vice president of Chip Design, building high-performance InfiniBand, Ethernet, and NVLink solutions that helped transform the data center industry and enable modern AI infrastructure. Most recently, Bukspan served as CEO of Pliops, a data acceleration technology company, where he led the organization's strategic direction and product development for KV-cache applications.

"Israel has been defining networking innovation for decades, from those formative years when we were proving what was possible to today's AI-driven transformation," said Ido Bukspan, vice president of ASIC Engineering at Astera Labs. "I see the same drive, the same intensity to deliver highly performant connectivity solutions at Astera Labs. Together, we're taking AI connectivity to the next level. Come join us."

To learn more about Astera Labs and apply for openings, visit www.asteralabs.com/careers/ or contact IsraelJobs@asteralabs.com.

About Astera Labs

Astera Labs (Nasdaq: ALAB) provides rack-scale AI infrastructure through purpose-built connectivity solutions. By collaborating with hyperscalers and ecosystem partners, Astera Labs enables organizations to unlock the full potential of modern AI. Astera Labs' Intelligent Connectivity Platform integrates CXL[®], Ethernet, NVLink Fusion, PCIe[®], and UALink[™] semiconductor-based technologies with the company's COSMOS software suite to unify diverse components into cohesive, flexible systems that deliver end-to-end scale-up, and scale-out connectivity. The company's custom connectivity solutions business complements its standards-based portfolio, enabling customers to deploy tailored architectures to meet their unique infrastructure requirements. Discover more at www.asteralabs.com.

Forward-Looking Statements

This communication contains certain forward-looking statements regarding Astera Labs' expectations with respect to its new Israel research and development (R&D) design center, including the center's vision, role, focus, leadership, talent strategy, and anticipated impact on technology and product development, R&D efforts, collaborations, and the adoption of its Intelligent Connectivity Platform. Forward-looking statements are generally identified by words such as "aims," "expects," "focuses," "looks," "will," and similar expressions or variations thereof.

These forward-looking statements involve risks and uncertainties, many of which are beyond Astera Labs' control, that could cause actual results to differ materially from those expressed or implied. Such risks and uncertainties include, among others, the possibility that the expectations, vision, and strategies related to the design center may not be realized; delays, disruptions, challenges, or increased costs associated with conducting advanced R&D and developing next-generation scale-up fabrics; the ability to identify, hire, integrate, and retain the talent necessary to support the center's objectives; competitive pressures; the complexities and uncertainties inherent in developing and deploying new solutions based on emerging features and technologies; litigation or disputes arising from activities related to the design center or associated talent; macroeconomic conditions, including general conditions affecting the semiconductor industry; regulatory restrictions; geopolitical events, policies, and conflicts; and other risks and uncertainties described in Astera Labs' filings with the U.S. Securities and Exchange Commission, including its most recent Forms 10-K and 10-Q.

Forward-looking statements speak only as of the date they are made. Readers are cautioned not to place undue reliance on these forward-looking statements. Astera Labs undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise, except as required by law.



Source: ASTERA LABS, INC.